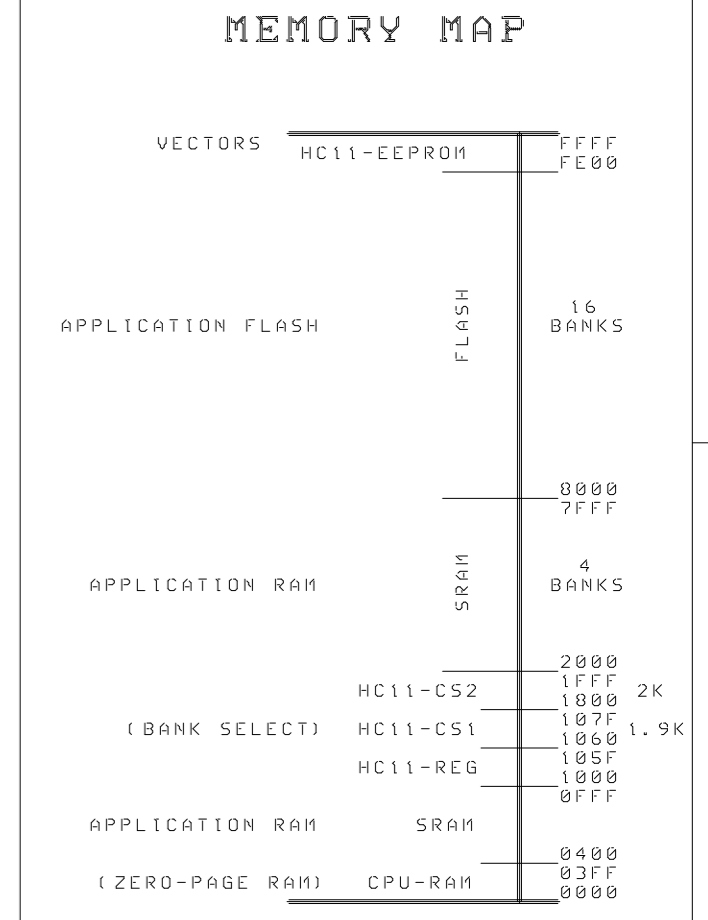


DATA TRANSLATION

DATA LINES ARE SWAPPED BETWEEN THE HC11 CPU AND THE OTHER DEVICES AS PER THE FOLLOWING CHART

HC11	SRAM	FLASH	LATCH	EXP.
D0	D7	D7	F15	PIN-19
D1	D0	D0	R17	PIN-24
D2	D6	D6	F17	PIN-20
D3	D5	D5	F16	PIN-21
D4	D4	D4	F18	PIN-22
D5	D3	D3	R15	PIN-23
D6	D2	D2	R18	PIN-26
D7	D1	D1	R16	PIN-25

R17 = SRAM CS2 R?? = SRAM
 F?? = FLASH



REVISIONS:
 12-MARCH-2003 CORRECT DATA TRANSLATION, ADD ADDRESS MAP

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Title CPU_3A2 SMD HC11 BOARD			
Size	Number	Revision	
A2		A	
Date:	12-MAR 2003	Sheet	1 of 1
File:	CPU_3A2/1	Drawn By:	PMB